OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
C2	SBCB	IMMED	2	2	D7	STB	DIRECT	4	2	E9	ADCB	INDEXED	4	2
C3	ADDD		4	3	D8	EORB		4	2	EA	ORB		4	2
C4	ANDB		2	2	D9	ADCB		4	2	EB	ADDB		4	2
C5	BITB		2	2	DA	ORB		4	2	EC	LDD		5	2
C6	LDB		2	2	DB	ADDB		4	2	ED	STD		5	2
C8	EORB		2	2	DC	LDD		5	2	EE	LDU		5	2
C9	ADCB		2	2	DD	STD		5	2	EF	STU	INDEXED	5	2
CA	ORB		2	2	DE	LDU		5	2	F0	SUBB	EXTENDED	5	3
CB	ADDB		2	2	DF	STU	DIRECT	5	2	F1	CMPB		5	3
CC	LDD		3	3	E0	SUBB	INDEXED	4	2	F2	SBCB		5	3
CE	LDU	IMMED	3	3	E1	CMPB		4	2	F3	ADDD		7	3
D0	SUBB	DIRECT	4	2	E2	SBCB		4	2	F4	ANDB		5	3
D1	CMPB		4	2	E3	ADDD		6	2	F5	BITB		5	3
D2	SBCB		4	2	E4	ANDB		4	2	F6	LDB		5	3
D3	ADDD		6	2	E5	BITB		4	2	F7	STB		5	3
D4	ANDB		4	2	E6	LDB		4	2	F8	EORB		5	3
D5	BITB		4	2	E7	STB		4	2	F9	ADCB		5	3
D6	LDB	DIRECT	4	2	E8	EORB	INDEXED	4	2	FA	ORB	EXTENDED	5	3

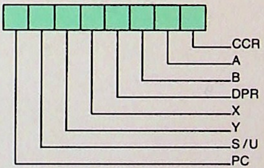
OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
FB	ADDB	EXTENDED	5	3	102E	LBGT	RELATIVE	5(6)	4	10CE	LDS	IMMED	4	4
FC	LDD		6	3	102F	LBLE	RELATIVE	5(6)	4	10DE	LDS	DIRECT	6	3
FD	STD		6	3	103F	SWI/2	INHERENT	20	2	10DF	STS	DIRECT	6	3
FE	LDU		6	3	1083	CMPD	IMMED	5	4	10EE	LDS	INDEXED	6	3
FF	STU	EXTENDED	6	3	108C	CMPY	↕	5	4	10EF	STS	INDEXED	6	3
1021	LBRN	RELATIVE	5	4	108E	LDY	IMMED	4	4	10FE	LDS	EXTENDED	7	4
1022	LBHI		5(6)	4	1093	CMPD	DIRECT	7	3	10FF	STS	EXTENDED	7	4
1023	LBLS		5(6)	4	109C	CMPY		7	3	113F	SWI/3	INHERENT	20	2
1024	LBHS/LBCC		5(6)	4	109E	LDY		6	3	1183	CMPU	IMMED	5	4
1025	LBCS/LBLO		5(6)	4	109F	STY	DIRECT	6	3	118C	CMPS	IMMED	5	4
1026	LBNE		5(6)	4	10A3	CMPD	INDEXED	7	3	1193	CMPU	DIRECT	7	3
1027	LBEQ		5(6)	4	10AC	CMPY		7	3	119C	CMPS	DIRECT	7	3
1028	LBVC		5(6)	4	10AE	LDY		6	3	11A3	CMPU	INDEXED	7	3
1029	LBVS		5(6)	4	10AF	STY	INDEXED	6	3	11AC	CMPS	INDEXED	7	3
102A	LBPL		5(6)	4	10B3	CMPD	EXTENDED	8	4	11B3	CMPU	EXTENDED	8	4
102B	LBMI		5(6)	4	10BC	CMPY		8	4	11BC	CMPS	EXTENDED	8	4
102C	LBGE		5(6)	4	10BE	LDY		7	4					
102D	LBLT	RELATIVE	5(6)	4	10BF	STY	EXTENDED	7	4					

12408 PRINTED IN USA 12-78 IMPERIAL LITHO B75703

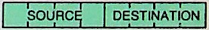
OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
44	LSRA	INHERENT	2	1	5D	TSTB	INHERENT	2	1	77	ASR	EXTENDED	7	3
46	RORA		2	1	5F	CLRB	INHERENT	2	1	78	ASL/LSL		7	3
47	ASRA		2	1	60	NEG	INDEXED	6	2	79	ROL		7	3
48	ASLA/LSLA		2	1	63	COM		6	2	7A	DEC		7	3
49	ROLA		2	1	64	LSR		6	2	7C	INC		7	3
4A	DECA		2	1	66	ROR		6	2	7D	TST		7	3
4C	INCA		2	1	67	ASR		6	2	7E	JMP		4	3
4D	TSTA		2	1	68	ASL/LSL		6	2	7F	CLR	EXTENDED	7	3
4F	CLRA		2	1	69	ROL		6	2	80	SUBA	IMMED	2	2
50	NEGB		2	1	6A	DEC		6	2	81	CMPA		2	2
53	COMB		2	1	6C	INC		6	2	82	SBCA		2	2
54	LSRB		2	1	6D	TST		6	2	83	SUBD		4	3
56	RORB		2	1	6E	JMP		3	2	84	ANDA		2	2
57	ASRA		2	1	6F	CLR	INDEXED	6	2	85	BITA		2	2
58	ASLB/LSLB		2	1	70	NEG	EXTENDED	7	3	86	LDA		2	2
59	ROLB		2	1	73	COM		7	3	88	EORA		2	2
5A	DECB		2	1	74	LSR		7	3	89	ADCA		2	2
5C	INCB	INHERENT	2	1	76	ROR	EXTENDED	7	3	8A	ORA	IMMED	2	2

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
8B	ADDA	IMMED	2	2	9E	LDX	DIRECT	5	2	B0	SUBA	EXTENDED	5	3
8C	CMPX	IMMED	4	3	9F	STX	DIRECT	5	2	B1	CMPA		5	3
8D	BSR	RELATIVE	7	2	A0	SUBA	INDEXED	4	2	B2	SBCA		5	3
8E	LDX	IMMED	3	3	A1	CMPA		4	2	B3	SUBD		7	3
90	SUBA	DIRECT	4	2	A2	SBCA		4	2	B4	ANDA		5	3
91	CMPA		4	2	A3	SUBD		6	2	B5	BITA		5	3
92	SBCA		4	2	A4	ANDA		4	2	B6	LDA		5	3
93	SUBD		6	2	A5	BITA		4	2	B7	STA		5	3
94	ANDA		4	2	A6	LDA		4	2	B8	EORA		5	3
95	BITA		4	2	A7	STA		4	2	B9	ADCA		5	3
96	LDA		4	2	A8	EORA		4	2	BA	ORA		5	3
97	STA		4	2	A9	ADCA		4	2	BB	ADDA		5	3
98	EORA		4	2	AA	ORA		4	2	BC	CMPX		7	3
99	ADCA		4	2	AB	ADDA		4	2	BD	JSR		8	3
9A	ORA		4	2	AC	CMPX		6	2	BE	LDX		6	3
9B	ADDA		4	2	AD	JSR		7	2	BF	STX	EXTENDED	6	3
9C	CMPX		6	2	AE	LDX		5	2	C0	SUBB	IMMED	2	2
9D	JSR	DIRECT	7	2	AF	STX	INDEXED	5	2	C1	CMPB	IMMED	2	2

PUSH/PULL POST BYTE



TRANSFER/EXCHANGE POST BYTE



REGISTER FIELD

0000 = D (A:B)	1000 = A
0001 = X	1001 = B
0010 = Y	1010 = CCR
0011 = U	1011 = DPR
0100 = S	
0101 = PC	

OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#	OP	MNEM	MODE	~	#
00	NEG	DIRECT	6	2	1C	ANDCC	IMMED	3	2	2E	BGT	RELATIVE	3	2
03	COM		6	2	1D	SEX	INHERENT	2	1	2F	BLE	RELATIVE	3	2
04	LSR		6	2	1E	EXG	↕	8	2	30	LEAX	INDEXED	4	2
06	ROR		6	2	1F	TFR	INHERENT	7	2	31	LEAY	↕	4	2
07	ASR		6	2	20	BRA	RELATIVE	3	2	32	LEAS		4	2
08	ASL/LSL		6	2	21	BRN		3	2	33	LEAU	INDEXED	4	2
09	ROL		6	2	22	BHI		3	2	34	PSHS	INHERENT	5	2
0A	DEC		6	2	23	BLS		3	2	35	PULS		5	2
0C	INC		6	2	24	BHS/BCC		3	2	36	PSHU		5	2
0D	TST		6	2	25	BLO/BCS		3	2	37	PULU		5	2
0E	JMP		3	2	26	BNE		3	2	39	RTS		5	1
0F	CLR	DIRECT	6	2	27	BEQ		3	2	3A	ABX		3	1
12	NOP	INHERENT	2	1	28	BVC		3	2	3B	RTI		6/15	1
13	SYNC	INHERENT	2	1	29	BVS		3	2	3C	CWAI		21	2
16	LBRA	RELATIVE	5	3	2A	BPL		3	2	3D	MUL		11	1
17	LBSR	RELATIVE	9	3	2B	BMI		3	2	3F	SWI		19	1
19	DAA	INHERENT	2	1	2C	BGE		3	2	40	NEGA		2	1
1A	ORCC	IMMED	3	2	2D	BLT	RELATIVE	3	2	43	COMA	INHERENT	2	1

↑
PUSH ORDER

BHI	BLS
BHS	BLO
BEQ	BNE
BLS	BHI
BLO	BHS

HEXADECIMAL AND DECIMAL CONVERSION

HOW TO USE THE TABLES

CONVERSION TO DECIMAL: Find the decimal weights for corresponding hexadecimal characters beginning with the least significant character. The sum of the decimal weight is the decimal value of the hexadecimal number.

CONVERSION TO HEXADECIMAL: Find the highest decimal value in the table which is lower than or equal to the decimal number to be converted. The corresponding hexadecimal character is the most significant character. Subtract the decimal value found from the decimal number to be converted. With the difference, repeat the process to find subsequent hexadecimal characters.

HEXADECIMAL AND DECIMAL CONVERSION							
15 BYTE 8				7 BYTE 0			
15 CHAR 12		11 CHAR 8		7 CHAR 4		3 CHAR 0	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0
1	4 096	1	256	1	16	1	1
2	8 192	2	512	2	32	2	2
3	12 288	3	768	3	48	3	3
4	16 384	4	1 024	4	64	4	4
5	20 480	5	1 280	5	80	5	5
6	24 576	6	1 536	6	96	6	6
7	28 672	7	1 792	7	112	7	7
8	32 768	8	2 048	8	128	8	8
9	36 864	9	2 304	9	144	9	9
A	40 960	A	2 560	A	160	A	10
B	45 056	B	2 816	B	176	B	11
C	49 152	C	3 072	C	192	C	12
D	53 248	D	3 328	D	208	D	13
E	57 344	E	3 584	E	224	E	14
F	61 440	F	3 840	F	240	F	15

POWERS OF TWO	
2^n	n
1	0
2	1
4	2
8	3
16	4
32	5
64	6
128	7
256	8
512	9
1,024	10
2,048	11
4,096	12
8,192	13
16,384	14
32,768	15
65,536	16
131,072	17
262,144	18
524,288	19
1,048,576	20

ASCII CHARACTER SET (7-BIT CODE)								
M.S. CHAR L.S. CHAR	0 000	1 001	2 010	3 011	4 100	5 101	6 110	7 111
0 0000	NUL	DLE	SP	0	@	P	`	p
1 0001	SOH	DC1	!	1	A	Q	a	q
2 0010	STX	DC2	"	2	B	R	b	r
3 0011	ETC	DC3	#	3	C	S	c	s
4 0100	EOT	DC4	$	4	D	T	d	t
5 0101	ENQ	NAK	%	5	E	U	e	u
6 0110	ACK	SYN	&	6	F	V	f	v
7 0111	BEL	ETB	'	7	G	W	g	w
8 1000	BS	CAN	(	8	H	X	h	x
9 1001	HT	EM	)	9	I	Y	i	y
A 1010	LF	SUB	*	:	J	Z	j	z
B 1011	VT	ESC	+	;	K	[	k	
C 1100	FF	FS	.	<	L	\	l	{
D 1101	CR	GS	-	=	M	]	m	
E 1110	SO	RS	●	>	N	↑	n	~
F 1111	SI	VS	/	?	O	—	o	DEL

INDEXED ADDRESSING POST BYTE REGISTER BIT ASSIGNMENTS

POST-BYTE REGISTER BIT								INDEXED ADDRESSING MODE
7	6	5	4	3	2	1	0	
0	X	X	X	X	X	X	X	EA = ,R ± 4 BIT OFFSET
1	X	X	0	0	0	0	0	,R+
1	X	X	X	0	0	0	1	,R++
1	X	X	0	0	0	1	0	,–R
1	X	X	X	0	0	1	1	,– –R
1	X	X	X	0	1	0	0	EA = ,R ± 0 OFFSET
1	X	X	X	0	1	0	1	EA = ,R ± ACCB OFFSET
1	X	X	X	0	1	1	0	EA = ,R ± ACCA OFFSET
1	X	X	X	1	0	0	0	EA = ,R ± 7 BIT OFFSET
1	X	X	X	1	0	0	1	EA = ,R ± 15 BIT OFFSET
1	X	X	X	1	0	1	1	EA = ,R ± D OFFSET)
1	X	X	X	1	1	0	0	EA = ,PC ± 7 BIT OFFSET
1	X	X	X	1	1	0	1	EA = ,PC ± 15 BIT OFFSET
1	X	X	1	1	1	1	1	EA = ,ADDRESS

ADDRESSING MODE FIELD

I FIELD
FOR B7 = 1: INDIRECT
FOR B7 = 0: SIGN BIT

REGISTER FIELD
00:R = X
01:R = Y
10:R = U
11:R = S

MC6809
MICROPROCESSOR

PRELIMINARY

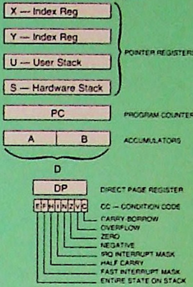
INSTRUCTION SET SUMMARY

MOTOROLA INC.
Integrated Circuit Division

3501 Ed Bluestein Blvd
Austin, Texas 78721
Telephone: (512) 928-6000

ISSUE A-1
NMOS MICROCOMPUTER SYSTEMS APPLICATIONS ENGINEERING
© Motorola, Inc., 1978

6809 PROGRAMMING MODEL



6809 STACKING ORDER

PULL ORDER
↓
CC
A
B
DP
X Hi
X Lo
Y Hi
Y Lo
U/S Hi
U/S Lo
PC Hi
PC Lo

INCREASING MEMORY
↓

6809 VECTORS	
FFFE	Restart
FFFC	NMI
FFFA	SWI
FFF8	IRQ
FFF6	FIRQ
FFF4	SWI2
FFF2	SWI3
FFF0	Reserved

Simple Conditional Branches

Condition	*Complement*
BEQ	BNE
BMI	BPL
BCS	BCC
BVS	BVC

Signed Conditional Branches

Condition	*Complement*
BGT	BLE
BGE	BLT
BEQ	BNE
BLE	BGT
BLT	BGE

Unsigned Conditional Branches

Condition	*Complement*

6809 ADDRESSING MODES

INSTRUCTION/ FORMS		INHERENT		DIRECT		EXTENDED		IMMEDIATE		INDEXED[1]		RELATIVE			5	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~[5]	#	DESCRIPTION	H	N	Z	V	C
ABX		3A	3	1													B + X → X (UNSIGNED)	•	•	•	•	•
ADC	ADCA				99	4	2	B9	5	3	B9	2	2	A9	4+	2+	A ← M + C + A	↕	↕	↕	↕	↕
	ADCR				D9	4	2	F9	5	3	C9	2	2	E9	4+	2+	B ← M + C → B	↕	↕	↕	↕	↕
ADD	ADDA				9B	4	2	BB	5	3	BB	2	2	AB	4+	2+	A ← M → A	↕	↕	↕	↕	↕
	ADDB				DB	4	2	FB	5	3	CB	2	2	EB	4+	2+	B ← M → B	↕	↕	↕	↕	↕
	ADDD				D3	6	2	F3	7	3	C3	4	3	E3	6+	2+	D ← M:M + 1 → D	•	↕	↕	↕	↕
AND	ANDA				94	4	2	B4	5	3	84	2	2	A4	4+	2+	A ∧ M → A	•	↕	↕	0	•
	ANDB				D4	4	2	F4	5	3	C4	2	2	E4	4+	2+	B ∧ M → B	•	↕	↕	0	•
	ANDCC										1C	3	2				CC ∧ IMM → CC	↕	↕	↕	↕	↕
ASL	ASLA	48	2	1													A, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
	ASLB	58	2	1													B, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
	ASL				08	6	2	78	7	3				68	6+	2+	M, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
ASR	ASRA	47	2	1													A, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	•	↕
	ASRB	57	2	1													B, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	•	↕
	ASR				07	6	2	77	7	3				67	6+	2+	M, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	•	↕
BCC	BCC													24	3	2	Branch C = 0	•	•	•	•	•
	LBCC													10 24	5(6)	4	Long Branch C = 0	•	•	•	•	•
BCS	BCS													25	3	2	Branch C = 1	•	•	•	•	•
	LBCS													10 25	5(6)	4	Long Branch C = 1	•	•	•	•	•
BEQ	BEQ													27	3	2	Branch Z = 0	•	•	•	•	•
	LBEQ													10 27	5(6)	4	Long Branch Z = 0	•	•	•	•	•
BGE	BGE													2C	3	2	Branch ≥ Zero	•	•	•	•	•
	LBGE													10 2C	5(6)	4	Long Branch ≥ Zero	•	•	•	•	•
BGT	BGT													2E	3	2	Branch > Zero	•	•	•	•	•
	LBGT													10 2E	5(6)	4	Long Branch > Zero	•	•	•	•	•
BHI	BHI													22	3	2	Branch Higher	•	•	•	•	•
	LBHI													10 22	5(6)	4	Long Branch Higher	•	•	•	•	•
BHS	BHS													24	3	2	Branch Higher or Same	•	•	•	•	•
	LBHS													10 24	5(6)	4	Long Branch Higher or Same	•	•	•	•	•
BIT	BITA				95	4	2	B5	5	3	85	2	2	A5	4+	2+	Bit Test A (M ∧ A)	•	↕	↕	0	•
	BITB				D5	4	2	F5	5	3	C5	2	2	E5	4+	2+	Bit Test B (M ∧ B)	•	↕	↕	0	•
BLE	BLE													2F	3	2	Branch ≤ Zero	•	•	•	•	•
	LBLE													10 2F	5(6)	4	Long Branch ≤ Zero	•	•	•	•	•

INSTRUCTION/ FORMS		INHERENT		DIRECT		EXTENDED		IMMEDIATE		INDEXED[1]		RELATIVE			5	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~[5]	#	DESCRIPTION	H	N	Z	V	C
BLO	BLO													25	3	2	Branch Lower	•	•	•	•	•
	LBLO													10 25	5(6)	4	Long Branch Lower	•	•	•	•	•
BLS	BLS													23	3	2	Branch Lower or Same	•	•	•	•	•
	LBLS													10 23	5(6)	4	Long Branch Lower or Same	•	•	•	•	•
BLT	BLT													2D	3	2	Branch < Zero	•	•	•	•	•
	LBLT													10 2D	5(6)	4	Long Branch < Zero	•	•	•	•	•
BMI	BMI													2B	3	2	Branch Minus	•	•	•	•	•
	LBMI													10 2B	5(6)	4	Long Branch Minus	•	•	•	•	•
BNE	BNE													26	3	2	Branch Z ≠ 0	•	•	•	•	•
	LBNE													10 26	5(6)	4	Long Branch Z ≠ 0	•	•	•	•	•
BPL	BPL													2A	3	2	Branch Plus	•	•	•	•	•
	LBPL													10 2A	5(6)	4	Long Branch Plus	•	•	•	•	•
BRA	BRA													20	3	2	Branch Always	•	•	•	•	•
	LBRA													16	5	3	Long Branch Always	•	•	•	•	•
BRN	BRN													21	3	2	Branch Never	•	•	•	•	•
	LBRN													10 21	5	4	Long Branch Never	•	•	•	•	•
BSR	BSR													8D	7	2	Branch to Subroutine	•	•	•	•	•
	LBSR													17	9	3	Long Branch to Subroutine	•	•	•	•	•
BVC	BVC													28	3	2	Branch V = 0	•	•	•	•	•
	LBVC													10 28	5(6)	4	Long Branch V = 0	•	•	•	•	•
BVS	BVS													29	3	2	Branch V = 1	•	•	•	•	•
	LBVS													10 29	5(6)	4	Long Branch V = 1	•	•	•	•	•
CLR	CLRA	4F	2	1													0 → A	•	0	1	0	0
	CLRB	5F	2	1													0 → B	•	0	1	0	0
	CLR				0F	6	2	7F	7	3				6F	6+	2+	0 → M	•	0	1	0	0
CMP	CMPA				91	4	2	B1	5	3	B1	2	2	A1	4+	2+	Compare M from A	↕	↕	↕	↕	↕
	CMPB				D1	4	2	F1	5	3	C1	2	2	E1	4+	2+	Compare M from B	↕	↕	↕	↕	↕
	CMPD				10 93	7	3	10 B3	8	4	10 B3	5	4	10 A3	7+	3+	Compare M:M + 1 from D	•	↕	↕	↕	↕
	CMPS				11 9C	7	3	11 BC	8	4	11 BC	5	4	11 AC	7+	3+	Compare M:M + 1 from S	•	↕	↕	↕	↕
	CMPU				11 83	7	3	11 B3	8	4	11 B3	5	4	11 A3	7+	3+	Compare M:M + 1 from U	•	↕	↕	↕	↕
	CMPX				9C	6	2	BC	7	3	8C	4	3	AC	6+	2+	Compare M:M + 1 from X	•	↕	↕	↕	↕
	CMPY				10 9C	7	3	10 BC	8	4	10 9C	5	4	10 AC	7+	3+	Compare M:M + 1 from Y	•	↕	↕	↕	↕

INSTRUCTION/ FORMS		INHERENT		DIRECT		EXTENDED		IMMEDIATE		INDEXED[1]		RELATIVE			5	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~[5]	#	DESCRIPTION	H	N	Z	V	C
COM	COMA	43	2	1													A → A	•	↕	↕	0	1
	COMB	53	2	1													B → B	•	↕	↕	0	1
	COM				03	6	2	73	7	3				63	6+	2+	M → M	•	↕	↕	0	1
CWAI		3C	20	2													CC ∧ IMM →CC, Wait for Interrupt	•	•	•	•	↕
DAA		19	2	1													Decimal Adjust A	•	↕	↕	↕	↕
DEC	DECA	4A	2	1													A − 1 → A	•	↕	↕	↕	•
	DECB	5A	2	1													B − 1 → B	•	↕	↕	↕	•
	DEC				0A	6	2	7A	7	3				6A	6+	2+	M − 1 → M	•	↕	↕	↕	•
EOR	EORA				98	4	2	B8	5	3	88	2	2	A8	4+	2+	A ⊻ M → A	•	↕	↕	0	•
	EORB				D8	4	2	F8	5	3	C8	2	2	E8	4+	2+	B ⊻ M → B	•	↕	↕	0	•
EXG	R1, R2	1E	7	2													R1 ↔ R2*	•	•	•	•	•
INC	INCA	4C	2	1													A + 1 → A	•	↕	↕	↕	•
	INCB	5C	2	1													B + 1 → B	•	↕	↕	↕	•
	INC				0C	6	2	7C	7	3				6C	6+	2+	M + 1 → M	•	↕	↕	↕	•
JMP					0E	3	2	7E	4	3				6E	3+	2+	EA* → PC	•	•	•	•	•
JSR					9D	7	2	BD	8	3				AD	7+	2+	Jump to Subroutine	•	•	•	•	•
LD	LDA				96	4	2	B6	5	3	86	2	2	A6	4+	2+	M → A	•	↕	↕	0	•
	LDB				D6	4	2	F6	5	3	C6	2	2	E6	4+	2+	M → B	•	↕	↕	0	•
	LDD				DC	5	2	FC	6	3	CC	3	3	EC	5+	2+	M:M + 1 → D	•	↕	↕	0	•
	LDS				10 DE	6	2	10 FE	7	4	10 CE	4	4	10 EE	6+	3+	M: M + 1 → S	•	↕	↕	0	•
	LDU				DE	5	2	FE	6	3	CE	3	3	EE	5+	2+	M: M + 1 → U	•	↕	↕	0	•
	LDX				9E	5	2	BE	6	3	8E	3	3	AE	5+	2+	M: M + 1 → X	•	↕	↕	0	•
	LDY				10 9E	6	3	10 BE	7	4	10 8E	4	4	10 AE	6+	3+	M: M + 1 → Y	•	↕	↕	0	•
LEA	LEAS													32	4+	2+	EA → S	•	•	•	•	•
	LEAU													33	4+	2+	EA → U	•	•	•	•	•
	LEAX													30	4+	2+	EA → X	•	•	↕	•	•
	LEAY													31	4+	2+	EA → Y	•	•	↕	•	•
LSL	LSLA	48	2	1													A, b7 b6 b5 b4 b3 b2 b1 b0 0	↕	↕	↕	↕	↕
	LSLB	58	2	1													B, b7 b6 b5 b4 b3 b2 b1 b0 0	↕	↕	↕	↕	↕
	LSL				08	6	2	78	7	3				68	6+	2+	M, b7 b6 b5 b4 b3 b2 b1 b0 0	↕	↕	↕	↕	↕
LSR	LSRA	44	2	1													A, 0 → b7 b6 b5 b4 b3 b2 b1 b0 C	•	0	↕	•	↕
	LSRB	54	2	1													B, 0 → b7 b6 b5 b4 b3 b2 b1 b0 C	•	0	↕	•	↕
	LSR				04	6	2	74	7	3				64	6+	2+	M, 0 → b7 b6 b5 b4 b3 b2 b1 b0 C	•	0	↕	•	↕
MUL		3D	11	1													A × B → D (Unsigned)	•	•	↕	•	↕
NEG	NEGA	40	2	1													A + 1 → A	↕	↕	↕	↕	↕
	NEGB	50	2	1													B + 1 → B	↕	↕	↕	↕	↕
	NEG				00	6	2	70	7	3				60	6+	2+	M + 1 → M	↕	↕	↕	↕	↕
NOP		12	2	1													No Operation	•	•	•	•	•
OR	ORA				9A	4	2	BA	5	3	8A	2	2	AA	4+	2+	A ⋁ M → A	•	↕	↕	0	•
	ORB				DA	4	2	FA	5	3	CA	2	2	EA	4+	2+	B ⋁ M → B	•	↕	↕	0	•
	ORCC										1A	3	2				CC ⋁ IMM → CC	↕	↕	↕	↕	↕
PSH	PSHS	34	5+	2													Push Registers on S Stack	•	•	•	•	•
	PSHU	36	5+	2													Push Registers on U Stack	•	•	•	•	•

INSTRUCTION/ FORMS		INHERENT		DIRECT		EXTENDED		IMMEDIATE		INDEXED[1]		RELATIVE			5	3	2	1	0
		OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~[5]	#	DESCRIPTION	H	N	Z	V	C
PUL	PULS	35	5+	2													Pull Registers from S Stack	•	•	•	•	•
	PULU	37	5+	2													Pull Registers from U Stack	•	•	•	•	•
ROL	ROLA	49	2	1													A, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
	ROLB	59	2	1													B, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
	ROL				09	6	2	79	7	3				69	6+	2+	M, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
ROR	RORA	46	2	1													A, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
	RORB	56	2	1													B, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
	ROR				06	6	2	76	7	3				66	6+	2+	M, b7 b6 b5 b4 b3 b2 b1 b0 C	↕	↕	↕	↕	↕
RTI		3B	6/15	1													Return From Interrupt	↕	↕	↕	↕	↕
RTS		39	5	1													Return From Subroutine	•	•	•	•	•
SBC	SBCA				92	4	2	B2	5	3	82	2	2	A2	4+	2+	A − M − C → A	↕	↕	↕	↕	↕
	SBCB				D2	4	2	F2	5	3	C2	2	2	E2	4+	2+	B − M − C → B	↕	↕	↕	↕	↕
SEX		1D	2	1													Sign Extend B into A	•	↕	↕	•	•
ST	STA				97	4	2	B7	5	3				A7	4+	2+	A → M	•	↕	↕	0	•
	STB				D7	4	2	F7	5	3				E7	4+	2+	B → M	•	↕	↕	0	•
	STD				DD	5	2	FD	6	3				ED	5+	2+	D → M: M + 1	•	↕	↕	0	•
	STS				10 DF	6	3	10 FF	7	4				10 EF	6+	3+	S → M: M + 1	•	↕	↕	0	•
	STU				DF	5	2	FF	6	3				EF	5+	2+	U → M: M + 1	•	↕	↕	0	•
	STX				9F	5	2	BF	6	3				AF	5+	2+	X → M: M + 1	•	↕	↕	0	•
	STY				10 9F	6	3	10 BF	7	4				10 AF	6+	3+	Y → M: M + 1	•	↕	↕	0	•
SUB	SUBA				90	4	2	B0	5	3	80	2	2	A0	4+	2+	A − M → A	↕	↕	↕	↕	↕
	SUBB				D0	4	2	F0	5	3	C0	2	2	E0	4+	2+	B − M → B	↕	↕	↕	↕	↕
	SUBD				93	6	2	B3	7	3	83	4	3	A3	6+	2+	D − M: M + 1 → D	•	↕	↕	↕	↕
SWI	SWI	3F	19	1													Software Interrupt 1	•	•	•	•	•
	SWI2*	10 3F	20	2													Software Interrupt 2	•	•	•	•	•
	SWI3*	11 3F	20	2													Software Interrupt 3	•	•	•	•	•
SYNC		13	>2	1													Synchronize to Interrupt	•	•	•	•	•
TFR	R1, R2	1F	7	2													R1 → R2*	•	•	•	•	•
TST	TSTA	4D	2	1													Test A	•	↕	↕	0	•
	TSTB	5D	2	1													Test B	•	↕	↕	0	•
	TST				0D	6	2	7D	7	3				6D	6+	2+	Test M	•	↕	↕	0	•

INDEXED ADDRESSING MODES

TYPE	FORMS	NON INDIRECT Assembler Form	NON INDIRECT Post-Byte OP Code	+	+ #	INDIRECT Assembler Form	INDIRECT Post-Byte OP Code	+	+ #
CONSTANT OFFSET FROM R	NO OFFSET	, R	1RR01100	0	0	[, R]	1RR01100	3	0
	5 BIT OFFSET	n, R	0RRnnnnn	1	1	defaults to 8-bit			
	8 BIT OFFSET	n, R	1RR01000	1	1	[n, R]	1RR01000	4	1
	16 BIT OFFSET	n, R	1RR01001	4	2	[n, R]	1RR01001	7	2
ACCUMULATOR OFFSET FROM R	A—REGISTER OFFSET	A, R	1RR01110	1	0	[A, R]	1RR01110	4	0
	B—REGISTER OFFSET	B, R	1RR01101	1	0	[B, R]	1RR01101	4	0
	D—REGISTER OFFSET	D, R	1RR01011	4	0	[D, R]	1RR01011	7	0
AUTO INCREMENT/DECREMENT R	INCREMENT BY 1	, R+	1RR00000	2	0	not allowed			
	INCREMENT BY 2	, R++	1RR00001	3	0	[, R++]	1RR00001	6	0
	DECREMENT BY 1	, −R	1RR00010	2	0	not allowed			
	DECREMENT BY 2	, −−R	1RR00011	3	0	[, −−R]	1RR00011	6	0
CONSTANT OFFSET FROM PC	8 BIT OFFSET	n, PCR	1XX01100	1	1	[n, PCR]	1XX11100	4	1
	16 BIT OFFSET	n, PCR	1XX01101	5	2	[n, PCR]	1XX11101	8	2
EXTENDED INDIRECT	16 BIT ADDRESS	—	—	–	–	[n]	10011111	5	2

R = X, Y, U, or S
X = DON'T CARE

NOTES:

1. Given in the table are the base cycles and byte counts. To determine the total cycles and byte counts add the values from the '6809 indexing modes' table.
2. R1 and R2 may be any pair of 8 bit or any pair of 16 bit registers.
   The 8 bit registers are: A, B, CC, DP
   The 16 bit registers are: X, Y, U, S, D, PC
3. EA is the effective address.
4. The PSH and PUL instructions require 5 cycles plus 1 cycle for each byte pushed or pulled.
5. 5(6) means: 5 cycles if branch not taken, 6 cycles if taken.
6. SWI sets I&F bits. SWI2 and SWI3 do not affect I&F.
7. Conditions Codes set as a direct result of the instruction.
8. Value of half-carry flag is undefined.
9. Special Case—Carry set if b7 is SET.

LEGEND:

OP	Operation Code (Hexadecimal);	Z	Zero (byte)
~	Number of MPU Cycles;	V	Overflow, 2's complement
#	Number of Program Bytes;	C	Carry from bit 7
+	Arithmetic Plus;	↕	Test and set if true, cleared otherwise
−	Arithmetic Minus;	•	Not Affected
*	Multiply	CC	Condition Code Register
M	Complement of M;	:	Concatenation
→	Transfer Into;	⋁	Logical or
H	Half-carry from bit 3;	∧	Logical and
N	Negative (sign bit)	⊻	Logical Exclusive or